WE CLAIM:

1. An apparatus for equalizing an input signal that has a pulse-width defined between a first edge and a second edge, comprising:

an equalizer circuit that produces an equalized signal in response to the input signal and an equalizer control signal such that the equalizer control signal selectively controls a characteristic of the equalizer to shape the equalized signal from the input signal;

a data slicer circuit that produces a data signal in response to the equalized signal, the data signal corresponding to a digital representation of the equalized signal;

a comparator circuit that produces a comparator output signal in response to a comparison between the equalized signal and a peak level signal;

a sampling circuit that samples data points within a sampling window in response to the comparator output signal and the data signal, the sampling window having edges that correspond to the pulse-width of the input signal; and

a digital control logic circuit that produces the equalizer control signal in response to a persistent condition that is determined from the sampled data points such that the equalizer control signal adjusts the equalizer in response to the persistent condition.

2. An apparatus as in Claim 1, wherein the characteristic of the equalizer is a gain of the equalizer such that the gain of the equalizer is responsive to the equalizer control signal.

3. An apparatus as in Claim 1, wherein the equalizer circuit includes a high pass filter that has a transfer function that is an inverse transfer function corresponding to cable loss characteristics such that the equalizer circuit reduces errors in the input signal.

4. An apparatus as in Claim 1, wherein the equalizer circuit has a predetermined number of equalizer settings that are responsive to the equalizer control signal, and the equalizer control signal includes control bits that correspond to the predetermined number of equalizer settings.

5. An apparatus as in Claim 1, further comprising a peak level adjustment circuit that is arranged to produce the peak level signal in response to an amplitude control signal, and the digital control logic circuit is arranged to produce the amplitude control signal in response to another persistent condition that is determined from the sampled data points such that the peak level signal is adjusted by the amplitude control signal in response to the another persistent condition.

6. An apparatus as in Claim 1, further comprising a peak detection circuit that produces the peak level signal in response to the equalized signal and an amplitude control signal.

7. An apparatus as in Claim 1, wherein the input signal is a differential input signal, the equalized signal is a differential equalized signal, the peak level signal is a differential peak level signal, and the comparator circuit is arranged to produce the comparator output signal in response to a comparison between the differential equalized signal and the differential peak level signal.

8. An apparatus as in Claim 1, wherein the equalized signal is a differential equalized signal that includes a top equalized signal and a bottom equalized signal, the peak level signal is a differential peak level signal that includes a top peak level signal and a bottom peak level signal, and the comparator circuit is arranged such that the comparator output signal is a first logic level when the top equalized signal exceeds the top peak level signal, the comparator output signal is the first logic level when the bottom equalized signal drops below the bottom peak level signal, and the comparator output signal is a second logic level that is different from the first logic level when the top equalized signal is below the top peak level signal and the bottom equalized signal is above the bottom peak level signal.

9. An apparatus as in Claim 1, wherein the equalized signal is a differential equalized signal including a top equalized signal and a bottom equalized signal, the peak level signal is a differential peak level signal including a top peak level signal and a bottom peak level signal, wherein the top peak level signal is produced by a top peak

detection circuit that includes a first peak detector and a first buffer amplifier, the bottom peak level signal is produced by a bottom peak detection circuit that includes a second peak detector and a second buffer amplifier, the first peak detector detecting a high-peak amplitude of the equalized top signal, the second peak detector detecting a low-peak amplitude of the equalized bottom signal, the first buffer amplifier produces the top peak level signal in response to the high-peak amplitude and an amplitude control signal, and the second buffer amplifier produces the bottom peak level signal in response to the low-peak amplitude and the amplitude control signal such that the amplitude control signal adjusts the levels of the top and bottom peak level signals.

10. An apparatus as in Claim 1, further comprising:

a peak detector that detects a peak amplitude of the equalized signal; and

a buffer amplifier that produces the peak level signal in response to the peak amplitude and a peak control signal such that the buffer amplifier scales the peak amplitude in response to the peak control signal to produce the peak level signal.

11. An apparatus as in Claim 10, wherein the buffer amplifier has a predetermined number of amplitude settings that are responsive to the peak control signal, and the peak control signal includes amplitude control bits that correspond to the predetermined number of amplitude settings.

12. An apparatus as in Claim 1, wherein the equalizer control signal is adjusted by the digital control logic circuit during at least one of an initial training time, a continuous time, and a periodic time interval.

13. An apparatus as in Claim 1, wherein the sampled data points include a first sampled data point and a second sampled data point, the first sampled data point corresponding to a sample of the output of the comparator after the first edge of the input signal, and the second sampled data point corresponding to another sample of the output of the comparator in response to the data signal such that the sampled data points correspond to sampled points from the equalized signal within the pulse-width of the input signal.

14. An apparatus as in Claim 13, wherein the persistent condition is an over-shoot condition when the first sampled data point indicates a first logic level and the second sampled data point indicates a second logic level that is different from the first logic level for a persistent time interval, the persistent condition is an under-shoot condition when the first sampled data point indicates the second logic level and the second sampled data point indicates the first logic level for the persistent time interval, wherein the digital logic circuit is arranged to adjust the equalizer control signal to compensate for the over-shoot and under-shoot conditions.

15. An apparatus as in Claim 13, wherein the persistent condition is an over-amplitude condition when the first sampled data point indicates a first logic level and the second sampled data point indicates the first logic level for a persistent time interval, the persistent condition is an under-amplitude condition when the first sampled data point indicates a second logic level that is different from the first logic level and the second sampled data point indicates the second logic level for the persistent time interval, wherein the digital logic circuit is arranged to adjust the peak level signal to compensate for the over-amplitude and under-amplitude conditions.

16. An apparatus as in Claim 1, wherein the digital control logic circuit includes a decoder logic circuit, a state logic circuit, a counter circuit, and an equalizer setting circuit, wherein the decoder logic circuit is arranged to evaluate the sampled data points to determine a current condition of the equalized signal, wherein the state logic circuit is arranged to control the counter circuit in response to the current condition and to adjust the characteristic of the equalizer such that equalizer settings are changed when a count of the counter circuit reaches a predetermined count level, the predetermined count level indicating that the current condition of the equalized signal is the persistent condition.

17. An apparatus as in Claim 16, wherein the equalizer setting circuit is arranged to produce at least one of an amplitude adjustment setting and an equalizer adjustment setting, wherein the amplitude adjustment setting is effective to control the

peak level signal, and the equalizer adjustment setting is effective to control the characteristic of the equalizer circuit.

18. An apparatus as in Claim 16, wherein the state logic circuit is arranged to increment the count of the counter circuit when the current condition is the same as a previous condition, and the state logic circuit is arranged to reset the count of the counter circuit when the current condition is an opposite condition to the previous condition.

19. An apparatus as in Claim 18, wherein the state logic circuit is arranged to reset the count of the counter circuit when the current condition is different from both the opposite condition and the previous condition.

20. An apparatus as in Claim 1, wherein the sampling circuit includes a timing delay circuit that produces a first timing signal and a second timing signal, and the sampling circuit produces the sampled data points in response to the first timing signal, the second timing signal and the output of the comparator, wherein the first timing signal is a first logic pulse that is responsive to rising and falling edges of the data signal, and the second timing signal is another logic pulse that occurs a predetermined time delay after one of the rising and falling edges of the data signal such that the logic pulse and the another logic pulse occur within the pulse-width of the input signal.

21. An apparatus as in Claim 20, wherein the comparator circuit includes a reset control input that is coupled to the first timing signal such that the output of the comparator is periodically reset to a first logic level, and the output of the comparator indicates a second logic level that is different from the first logic level when the equalized signal exceeds the peak level signal.

22. An apparatus as in Claim 21, wherein the digital control logic circuit further comprising:

a first logic circuit that includes a first output signal that is periodically reset to the first logic level in response to the second timing signal, the first output signal

indicating the second logic level when the output of the comparator changes from the first logic level to the second logic level;

a second logic circuit that includes a second output signal that follows the first output signal in response to the first timing signal;

a third logic circuit that includes a third output signal that follows the second output signal in response to the second timing signal, wherein the third output signal corresponds to a first of the sampled data points; and

a fourth logic circuit that includes a fourth output signal that follows the output of the comparator in response to the second timing signal, wherein the fourth output signal corresponds to a second of the sampled data points.

23. A method for equalizing an input signal that has a pulse-width defined between a first edge and a second edge, comprising:

equalizing the input signal to produce an equalized signal;

comparing the equalized signal to a peak level to produce a comparator output;

sampling a first data point from the comparator output;

sampling a second data point from the comparator output, wherein the first and second data points correspond to sampled points that are within the pulse-width of the input signal;

analyzing the first and second data points to determine a condition of the equalized signal;

analyzing the condition of the equalized signal to determine when a persistent condition on the equalized signal exists; and

adjusting equalization settings of the equalizer in response to a persistent condition that persists for a predetermined interval such that the input signal is properly equalized.

24. A method as in Claim 23, analyzing the first and second data points further comprising:

detecting an over-amplitude condition when the first and second data points indicate a first logic level;

detecting an under-amplitude condition when the first and second data points indicate a second logic level that is different from the first logic level;

detecting an over-shoot condition when the first data point indicates the first logic level and the second data point indicates the second logic level; and

detecting an under-shoot condition when the first data point indicates the second logic level and the second data point indicates the first logic level.

25. A method as in Claim 23, analyzing the condition of the equalized signal further comprising:

analyzing the first and second data points from a first sample time;

analyzing the first and second data points from a second sample time that is subsequent to the first sample time;

comparing the first data point from the first sample time to the first data point from the second sample time to produce a first point comparison; and

comparing the second data point from the first sample time to the second data point from the second sample time to produce a second point comparison.

26. A method as in Claim 25, further comprising:

increasing a persistence counter when the first point comparison and the second point comparison indicate that the first and second data points are unchanged form the first sample time to the second sample time; and

resetting the persistence counter when at least one of the first point comparison and the second point comparison indicates that at least one of the first and second data points have changed form the first sample time to the second sample time.

27. A method as in Claim 25, further comprising:

detecting an over-amplitude condition when the first and second data points indicate a first logic level;

detecting an under-amplitude condition when the first and second data points indicate a second logic level that is different from the first logic level, wherein the under-amplitude condition is an opposite condition to the over-amplitude condition;

detecting a first other condition when the first data point and the second data point indicates the condition of the equalized signal is other than the over-amplitude condition and the under-amplitude condition; and

storing a first previous signal condition that corresponds to the condition of the equalized signal from the first sample time, wherein the first previous signal condition corresponds to one of the over-amplitude condition and the under-amplitude condition;

increasing a first persistence counter when the condition of the equalized signal from the second sample time corresponds to the first previous signal condition; and

resetting the first persistence counter when the condition of the equalized signal from the second sample time corresponds to the opposite condition to the first previous signal condition.

28. A method as in Claim 25, further comprising:

detecting an over-shoot condition when the first data point indicates the first logic level and the second data point indicates the second logic level; and

detecting an under-shoot condition when the first data point indicates the second logic level and the second data point indicates the first logic level, wherein the under-shoot condition is an opposite condition to the over-shoot condition;

detecting a second other condition when the first data point and the second data point indicates the condition of the equalized signal is other than the over-shoot condition and the under-shoot condition; and

storing a second previous signal condition that corresponds to the condition of the equalized signal from the first sample time, wherein the second previous signal condition corresponds to one of the over-shoot condition and the under-shoot condition;

increasing a second persistence counter when the condition of the equalized signal from the second sample time corresponds to the second previous signal condition; and

resetting the second persistence counter when the condition of the equalized signal from the second sample time corresponds to the opposite condition to the second previous signal condition.

29. A method as in Claim 26, further comprising resetting the first persistence counter when the condition of the equalized signal from the second sample time corresponds to the first other condition.

30. A method as in Claim 27, further comprising resetting the second persistence counter when the condition of the equalized signal from the second sample time corresponds to the second other condition.

31. A method as in Claim 27, further comprising:

determining when the persistence counter has reached a predetermined count level;

adjusting the equalization setting of the equalizer in response to a first type of persistent condition when the predetermined count level corresponds to a first predetermined interval;

adjusting the peak level in response to a second type of persistent condition when the predetermined count level corresponds to the second predetermined interval; and

resetting the persistence counter after completing the adjustments to at least one of the equalization setting and the peak level, whereby the equalization of the input signal is adjusted by adjusting the peak level and the equalization level.

32. A method as in Claim 23, further comprising adjusting other equalization settings of another equalizer in response to the persistent condition wherein the equalization settings and the other equalization settings are the same such that an other

input signal is equalized by the other equalizer similar to the input signal that is equalized by the equalizer.

33. An equalization system that includes a first sample point and a second sample point from an input signal that has a pulse-width defined between a first edge and a second edge, comprising:

a means for equalizing the input signal produces an equalized signal in response to the input signal and an equalization control signal;

a means for comparing produces a comparator output signal in response to a comparison between the equalized signal and a peak level signal;

a means for sampling samples the comparator output to produce the first sample point and the second sample point in response to the equalized signal and the comparator output signal, the first sample point corresponding to a sample of the comparator output signal after the first edge of the input signal, and the second sample point corresponding to another sample of the comparator output signal; and

a means for adjusting adjusts at least one of the peak level signal and the equalization control signal in response to the first sample point and the second sample point such that equalization of the input signal is adjusted.

34. An apparatus as in Claim 33, further comprising:

a means for analyzing determines a condition of the equalized signal by analyzing the first sample point and the second sample point; and

a means for determining persistence determines when the condition of the equalized signal becomes a persistent condition.

35. An apparatus as in Claim 33, wherein the condition is at least one of an over-amplitude condition, an under-amplitude condition, an over-shoot condition, and an under-shoot condition.

36. An apparatus as in Claim 33, wherein the condition of the equalized signal is persistent when the condition has continued for a predetermined number of consecutive occurrences.

37. An apparatus as in Claim 33, further comprising:

a means for increasing an equalization level adjusts the equalization control signal such that the equalization level is increased when the under-shoot condition is persistent; and

a means for decreasing the equalization adjusts the equalization control signal such that the equalization level is decreased when the over-shoot condition is persistent.

38. An apparatus as in Claim 33, further comprising:

a means for increasing the peak level signal that increases the peak level signal when the under-amplitude condition is persistent; and

a means for decreasing the peak level signal that decreases the peak level signal when the over-amplitude condition is the persistent condition.